

**IN THE ABSTRACT OF THE DISCLOSURE:**

Please amend the abstract as follows:

**ABSTRACT OF THE DISCLOSURE**

~~The present invention provides a~~ A semiconductor integrated circuit is  
provided in which ~~a~~ the timing margin for fetching data is prevented from being  
reduced even in the case where the duty ratio of a clock signal is different from 50%.

The semiconductor integrated circuit includes: a clock input terminal for receiving a  
clock signal; a data input terminal for receiving a data signal; internal clock  
generating circuits for generating an internal clock signal which is switched at an  
intermediate timing between the i-th (i: an integer of 1 or larger) switch timing and  
the (i+1)th switch timing of the clock signal; and a latch circuit for latching the data  
signal synchronously with the internal clock signal. An internal clock signal which is  
switched at an intermediate timing between the i-th switch timing and the (i+1)th  
switch timing of the clock signal is generated, and the data signal is fetched  
synchronously with the internal clock signal.